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Deterministic Vision: Offloading Real-Time Camera Pipelines to FreeRTOS on Heterogeneous SoCs

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ABOUT ME

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Hi, I'm Akshay Shripati Abdar, currently working as an Embedded Software Engineer at Texas Instruments India. Beyond work I like to Travel, explore food, football & Gym

CURRENT FOCUS

Vision AI/ADAS SDK
EdgeAI SDK

PLATFORM

AM62A SoC
Heterogenous edge compute

EDUCATION

Mtech IIT Kharagpur 2024 in Embedded Controls & Software

About us: TI Processors and Open source









Decades of contribution and collaboration

Ingrained culture to give back to the community



Upstream FIRST!



Focus on long term, sustainable and quality products





Upstream and opensource ecosystem in device architecture







Upstream FIRST mentality!





Disclaimers

- This is a technology presentation, not product-readiness or roadmap commitment
- Opinions presented here are that of the speakers and may not reflect that of Texas Instruments Inc.
- Performance data is based on measured results.

Problem Statement

- Automotive DMS/OMS systems demand deterministic, real-time camera capture and vision processing
- Linux and RT-Linux cannot provide provable, auditable scheduling guarantees required by ISO 26262





Source: https://share.google/images/8rKMnmDa9x083v6OG

Key Challenge:

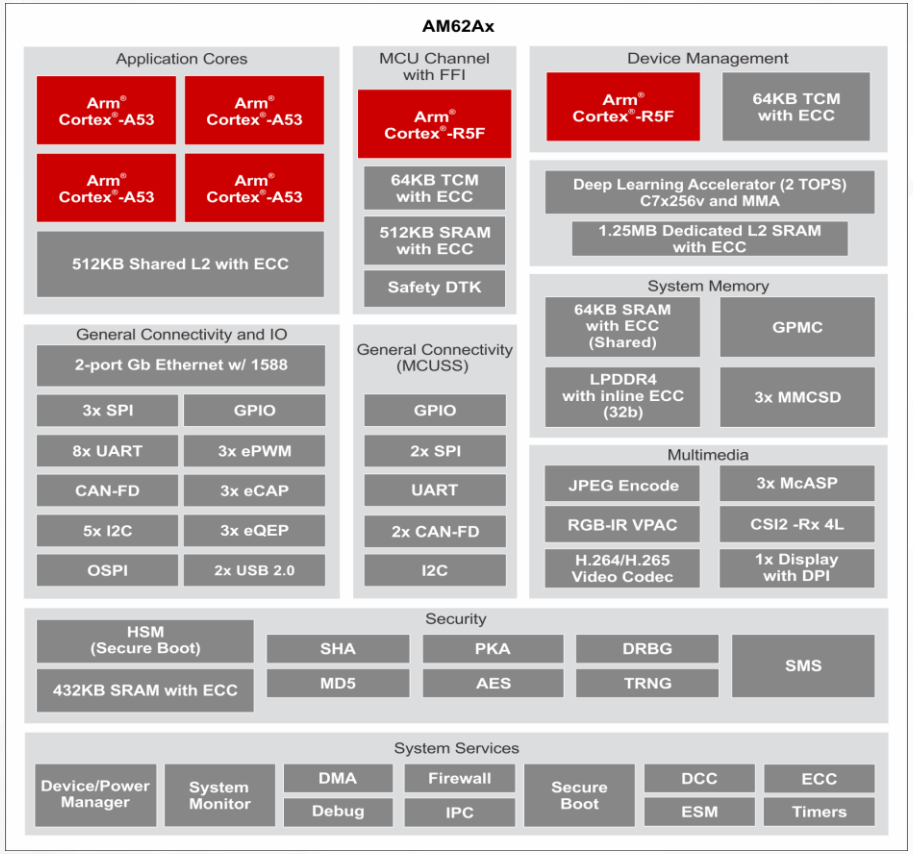
- Combine deterministic **Real-Time** guarantees (**Safety**)
- Complex **Image Processing Power** (**Functionality**)
- Maintaining **Certifiable System Architecture** (**ASIL-D**)

OS Trade-offs for Safety-Critical DMS/OMS

Criteria	Linux Flexible, Feature Rich.	RT Linux Real-Time Extensions	FreeRTOS Small. Simple. Real-Time
Pre-emption Model	Unpredictable	Improved Preemption	Priority-based
Latency Bound	Not Hard Real-Time	Improved Latency	Bounded/ Predictable
Certifiable	No	No	Yes
DMS/OMS Ready?	No	No	Yes

Takeaway: Use **Linux** for rich ecosystems, **RT-Linux** for Real-time on application processors and **FreeRTOS** for safety driven, deterministic **DMS/OMS** applications

AM62A SoC Architecture



Key Components:

A53 Application Core

- 4x ARM Cortex-A53 @ 1.4 GHz
- Runs Linux/QNX (User Applications)
- DMS/OMS application runs here

DM R5F (Device Manager)

- 1x ARM Cortex-R5F @ 400 MHz
- Runs FreeRTOS
- Handles Camera Capture,2A (AE/AWB), VPAC, Power/Clocks (DM)

MCU R5F

- AUTOSAR/Safety Reserved

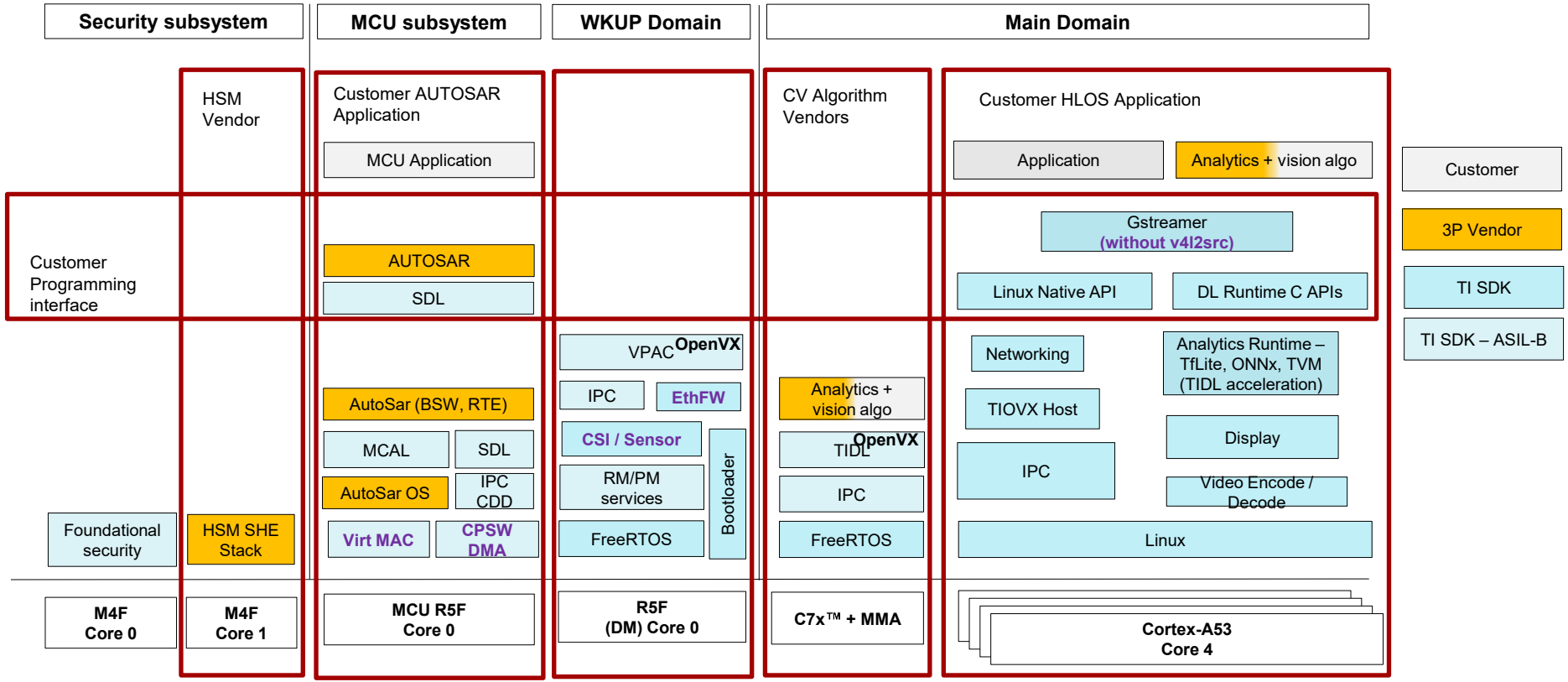
Accelerators + Interfaces

- CSIRX: Camera input (MIPI CSI-2)
- VPAC: Image processing (VISS, LDC, MSC)
- C7x™ + MMA: AI/ML DSP

Note: Both **DM R5F** and **C7x** core run FreeRtos on them

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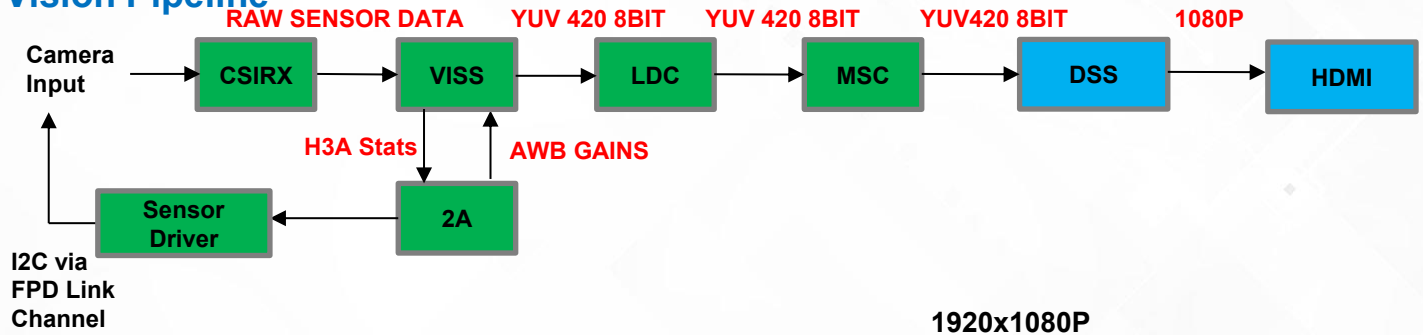
AM62A | Software Architecture – (Linux + FreeRTOS)



TIOVX Based Vision Pipeline

- The software architecture shown below demonstrates the distribution of tasks on different cores of AM62A both for **TI OpenVX (TIOVX)** based **Vision pipeline** and **Vision+AI** Pipeline
- TIOVX is TI's open-source OpenVX implementation for heterogeneous compute graphs

Vision Pipeline

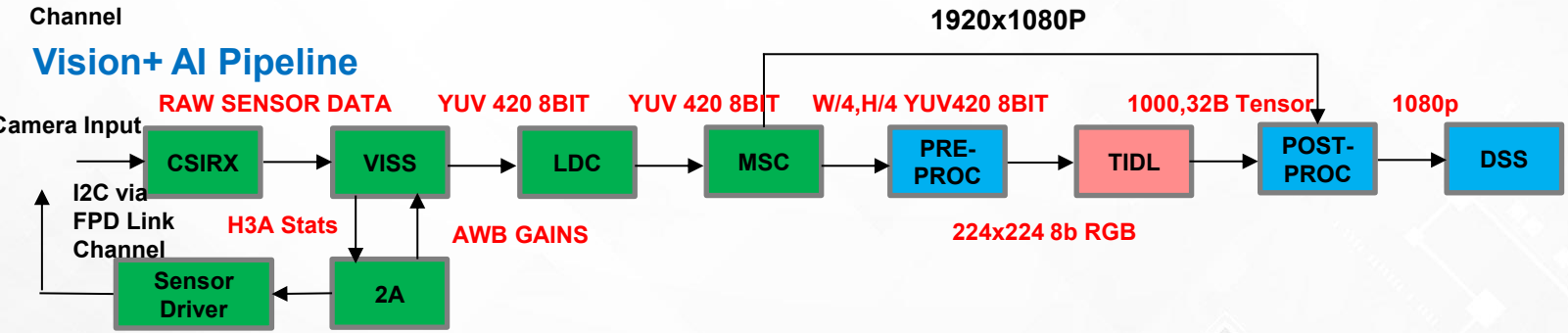


NODE ON R5F

NODE ON A53

NODE ON C7X™

Vision+ AI Pipeline



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Demo Video

Single camera demo using IMX390 Camera sensor



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Performance Numbers

A) Using 2MP IMX390

Metric	Single camera (Vision only)	OD Camera (Vision+AI)
1. R5F CPU Load 2. A53 CPU Load 3. C7x™ CPU Load	1. 20.15% 2. 7.76% 3. 0%	1. 5.57% 2. 8.14% 3. 32.29% (AI)
FPS Achieved	60 FPS	30 FPS
1. VISS Load 2. LDC Load 3. MSC Load	1. 36.30% 2. 33.78% 3. 34.68%	1. 18.66% 2. 17.35% 3. 52.84%
DDR PEAK BW (Read+Write)	8,675 MB/s	8,528 MB/s

B) Using 0X5C(5MP) Benchmark Sensor

Scenario	Max. DM R5F Load (%)
Device Manager(DM)task	~5%
DM Task + Single stream: Omnivision X5C sensor + 2A (AE/AWB)	~30%
DM Task + Single stream: Omnivision X5C sensor + 2A (AE/AWB)+ EthFWserver (with gPTP service)	~35%
DM Task + Single stream: Omnivision X5C sensor + 2A (AE/AWB)+ EthFWserver (with gPTP service)+ ping flood	~40%

Why This Architecture is Safe for ASIL-B/D Certification

ISO 26262 ASIL-B/D demands

Deterministic Behaviour

- Consistent, predictable execution
- No random timing variations
- Bounded worst-case latency
- Provable deadline achievement

Proof:

- VISS: 6321-6479us (2.5% variance
- LDC: 5649-5777us (2.3% variance)
- MSC: 5800-5929us (2.2% variance)
- Consistent hardware execution, measurable and predictable

No Task Starvation

- All critical tasks get CPU time
- No high-priority tasks blocking others
- Fair scheduling
- Guaranteed Service

Proof:

- FreeRTOS blocking mechanism
- Lower priority tasks run when higher blocks
- CAPTURE (Pri 15) never starves VISS (Pri 13)
- Every task guaranteed execution

Bounded Latency

- No unbounded delays
- Deadline guaranteed

Proof:

- Frame time: 16.66ms average
- Min: 15.98ms Max: 29.01ms Deadline: 33ms
- Margin: ~4ms minimum guaranteed

Key: Minimum frame drops, consistent timing across runs

Reliable Hardware Execution

- Hardware with fixed pipelines
- Consistent performance
- Predictable throughput

Proof:

- VPAC has dedicated hardware pipelines
- No A53 overhead and Linux can carry out other service tasks
- With maximum loading on R5F, we have 60% headroom

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Key Takeaways

- Bridges the gap - between general-purpose Linux and dedicated safety systems
  - Worst case latency on Linux is unpredictable to preemption. FreeRTOS on R5F can guarantee deadline compliance for safety functions
- Solves A53 Overloading as mixing camera capture with application logic on main processor causes unacceptable latency due to IPC overhead
- Proper utilization of DM R5F core by consolidating different tasks and functionalities on one single core.
- 40% Load, 60% Headroom - all services (**Capture + VPAC + DM + EthFW + gPTP**) run at only ~40% peak, leaving room for future workloads

Future Work

Future work targets On-The-Fly CSI-RX to VPAC path to eliminate DDR roundtrips.

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References

- AM62A SoC
- AM62A Datasheet
- AM62A Technical Reference Manual
- TIOVX User Guide
- TIDL User Guide
- EthFW User Guide

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Q&A

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